Master Thesis @ Ericsson

Dynamic Scheduling of Shared Hardware Resources, Optimized for deadlines and Low Latency using ML/AI

Background

In order to meet the demands of 5G which requires microsecond resolution in scheduling, Ericsson uses a tailor-made solution known as Ericsson Many-Core Architecture, EMCA [1].

’ Ericsson uses tailor-made Application Specific Integrated Circuits (ASIC), containing hundreds of specialized signal processors (DSPs) and accelerators, to implement the EMCA System on a Chip (SoC). SoC is an advanced ASIC with digital logic, mixed signal content, and processors.’

In this kind of system there are many concurrent jobs in different resource pools and there are also chaining of jobs between the resource pools. Before considering this advanced topic, let’s consider a more basic single core single job environment, where the basics of scheduling for a deadline is quite simple to understand. Start the job at a certain time and finish it before the deadline and you will be successful. In other words, there should be enough margin for the job to finish relative to the deadline when starting the job.

However, given the fact that the solution will run in many products and environments and adding a few more parameters make it more complicated:

- The job execution time, periodicity, deadline, and number of jobs in the system will change based on deployment and configuration
- The job runs in a multi-core environment with other concurrent jobs
- Some jobs in the pool have strict deadlines and some jobs more relaxed deadlines

The product will run in both TDD (time division duplex) and FDD (frequency division duplex), which allows DL(downlink) and UL(uplink) jobs to either switch running over time (TDD) or run side-by-side (FDD). For TDD, when switching from UL to DL adds another complexity where the jobs will run concurrently for a transient of time, seen as a peak load in the system. If there are not enough cores to execute the number of requested jobs, the jobs will wait for their turn in a queue.

Finally, to successfully run the 5G signal processing, various parts of the algorithm run in different resource pools, and the end time for one pool will be the start time for the next pool. The sum of all job times, and eventual wait times for the worst case is seen as the worst-case latency. The worst-case latency should be as small as possible to reliably be able to control the real time system over the air with 5G [2]. For the solution to fit all these environments and configurations, predictive or learning based algorithms are needed.

[1] https://www.ericsson.com/en/blog/2020/9/case-for-integrated-high-performance-ran-processing

[2] https://www.ericsson.com/en/networks/cases/accelerate-factory-automation-with-5g-urllc

There has been initial work done in this area to build up a simulation environment in python using simPy, with initial Q-learning and deep Q-learning-based Reinforcement Learning (RL) algorithms. [3]. In this thesis we look to improve and extend the initial work.

Scope/Objective

- Evaluate and improve the Q-learning reward function.
- Evaluate and improve the Q-learning model, state- and action space.
- Evaluate and improve exploration, can the system protect itself from deadline misses while exploring?
- Try to reduce the time-axis in the model to save memory for a real implementation. How big must the model be before the pattern is repeated?
- Can any extensions to the Q-learning be added, model based RL, decision tree, etc.?

Required qualifications

We are searching for two students with knowledge within automatic control, computer science, electrical engineering, or related field. The students should be eager to learn and explore new things. Prior experience of machine learning, reinforcement learning and python are an advantage.

[3]https://lup.lub.lu.se/luur/download?func=downloadFile&recordOId=9059466&fileOId=9059470

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